Remarks

Applicant has amended claims 1, 25, 40 and 44, and cancelled claims 14-24. Applicant respectfully submits that no new matter was added by the amendment, as all of the amended matter was either previously illustrated or described in the drawings, written specification and/or claims of the present application. Entry of the amendment and favorable consideration thereof is earnestly requested.

The examiner has rejected claims 1, 3-7 and 25-43 under 35 U.S.C. §102(b) as being unpatentable over U.S. Patent No. 6,274,871 to Dukor ("the '871 patent") in view of U.S. Patent No. 5,512,749 to Iddan ("the '749 patent"). The examiner has further rejected claims 8-13 under 35 U.S.C. §103(a) as being unpatentable over the '871 patent in view of the '749 patent and further in view of U.S. Patent No. 5,712,685 to Dumas ("the '685 patent"). The examiner has still further rejected claims 14-19 as being unpatentable over the '749 patent. The examiner has yet further rejected claims 20-24 as being unpatentable over the '749 patent in view of the '685 patent. Finally, the examiner has rejected claim 44 under 35 U.S.C. §103(a) as being unpatentable over the '871 patent in view of the '749 patent and further in view of U.S. Patent No. 5,123,953 to Harris ("the '953 patent"). These rejections are respectfully traversed.

Presently claims 1, 25, 40 and 44 each require among other elements "the outputs of the detector elements being directly fed in parallel to processing circuitry for image processing of the detector element outputs, each detector element having its own associated detection circuitry." The examiner has submitted that the '871 patent "does not specify that the outputs of the detector elements are fed in parallel to a processing means." The examiner has however submitted that the '749 patent discloses:

> - "the outputs of the detector elements (see figure 4) being fed in parallel (see figure 4, elements 106, 107, 108 to processing means (107 or 108) for processing the detector element outputs" and "parallel processing of detector elements of an FPA is well known in the art." (Official Action p. 3, lines 1-8)

Applicant respectfully disagrees. Rather, the '749 patent teaches that the "IR detector 20 comprises a two dimensional (2D) array 46 of , but not limited to, 128 X 128 or 256 X 256 IR sensitive elements 48 for producing electric signal having intensites proportional to the IR energy impinging thereon." (col. 4, lines 17-21). This is a very large number of detector elements to be processed that must be multiplexed prior to transmission to the image processor, which contravenes the teachings and desired outcome of this application. For instance, the '749 patent teaches that "[p]rocessing means 22 includes a processor 50 underlying IR detector 20 for multiplexing and amplifying the signals from IR sensitive elements 48 before their transmission thereto" and that "[p]rocessor 50 is situated at the focal plane of optics channel 18 and is known in the art as a focal plane processor (FPP)." (col. 4, lines 25-30) (emphasis added). Alternatively, in figure 4 the "signals from even and odd IR sensitive elements 106 are amplified by FFPs 107 and 108, respectively, before transmission to processing means 122." Therefore, both embodiments utilize FPPs located below an array of sensors, the embodiment in Figure 2 using one FPP (50) and the embodiment in Figure 4 utilizing two FPPs (107, 108). While the outputs of the IR detectors (106) in the second embodiment are parallel fed to FPPs (107, 108), the sole purpose for these devices is to multiplex and amplify the signals prior to transmission to processing means 122 where the image signals are processed. This type of system was described in the background of the invention where it stated that "[a]lthough such large arrays offer the advantage of speed of measurement through the acquisition of many pixels in parallel, currently available devices suffer from a loss of signal/noise ratio when compared with the projected performance based on a signal array element" and that the "loss arises from inefficiencies incurred in the multiplexing needed to handle the signal from such a large number of elements." (p. 3, lines 11-16). This is exactly the system taught in the '749 patent.

Alternatively, the present invention as claimed requires "the outputs of the detector elements being directly fed in parallel to processing circuitry for image processing of the detector element outputs, each detector element having its own associated detec-

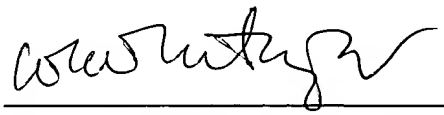
tion circuitry." This system as claimed will not suffer from the reduced signal to noise ratio inherent in the system disclosed and taught in the '749 patent because the outputs are individually and directly fed in parallel to processing circuitry without being multiplexed. Applicant has further amended claims 1, 25, 40 and 44 to include image processing to further clarify the invention as opposed to the '749 patent where the outputs are parallel fed to FPPs (107, 108) for multiplexing and amplification prior to transmission to processing means 122 where the image signals are then processed.

Applicant therefore respectfully submits that while parallel feeding of detector outputs to an FPP is known in the art, parallel feeding of detector elements to an image processor and parallel processing of image signals is not known in the art as multiplexed signals are not parallel processed.

Therefore, because neither the '871 patent nor the '749 patent teach, disclose or suggest outputs of the detector elements being directly fed in parallel to processing circuitry for image processing of the detector element outputs, each detector element having its own associated detection circuitry as required by claims 1, 25, 40 and 44, neither reference alone or in combination can render the present claims obvious.

Applicant therefore respectfully submits that claims 1, 3-13, and 25-44, all the claims remaining in the application, are in order for allowance and notice to that effect is respectfully requested.

Respectfully submitted,



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